

Application No.: 09/954799

Docket No.: SMQ-068

**REMARKS**

Applicants note with appreciation the indication of allowable subject matter in the instant application, namely, the subject matter recited in Claims 2-7, 9, 11, 13-20 and 24. Now in the application are Claims 1-24 of which Claims 1 and 12 are independent. No new matter has been added. The following comments address all stated grounds for rejection, and place the presently pending claims, as identified above, in condition for allowance.

**A. Rejection of Claims under 35 U.S.C. § 102(e)**

Claims 1 and 12 stand rejected under 35 U.S.C. § 102(e). For ease of the discussion below, the rejection of claims 1 and 12 under 35 U.S.C. § 102(e) are discussed separately.

**A1. Rejection of Claim 1 under 35 U.S.C. § 102(e)**

Claims 1 stands rejected under 35 U.S.C. § 102(e) as being anticipated in view of U.S. Publication No. 2002/0003453 of Segawa *et al.* (hereinafter "Segawa"). Applicants respectfully traverse this rejection and contend that Segawa does not anticipate claim 1.

Claim 1 is directed to an apparatus for receiving data of a source synchronous signal and a source synchronous clock signal in a source synchronous point to point communication system. The apparatus includes a receiver circuit for receiving the data of the source synchronous signal and a feedback circuit for providing the receiver with a plurality of feedback signals based on an output of the receiver circuit to synchronize receipt of the data of the source synchronous signal by the receiver circuit. Segawa does not anticipate claim 1.

Segawa discloses a PLL architecture that enables a PLL's VCO output signal, once phase locked with a carrier signal, to remain phase locked to the phase of said carrier signal despite the loss of said carrier signal. More specifically, Segawa discloses a carrier signal providing a serial stream of data. In contrast, a source synchronous point-to-point communication system receives data in parallel. Hence, the PLL as disclosed by Segawa is not an apparatus for receiving data of source synchronous signal in a source synchronous point-to-point communication system.

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The cited paragraph 0016 and figure 9 of Segawa disclose clock 1 as a reference signal used to detect the absence of the carrier signal through the use of a carrier detector. More specifically, in the event that said carrier signal is lost, the carrier detector acts as a mode selector that causes the PLL to switch from a carrier signal input to a reference voltage to prevent the VCO output from changing phase. Applicant's invention has a structure, a function and an operation different from the structure, the function and the operation of the PLL of Segawa. That is, the Applicant's invention discloses a source synchronous point-to-point communication system, which requires the transmitting device to provide a source synchronous clock for timing purposes by the receiving electronic device to receive data of said source synchronous source as described in the background of the invention found on page 1, lines 23-27 of the application.

Notwithstanding the above, for the sake of argument, even if the phase detector disclosed by Segawa could be characterized as the receiver circuit of the claimed invention, the feedback signal of Segawa that is based on the VCO output does not return to the phase detector. That is, unlike the phase detector of Segawa, the present invention requires a feedback circuit for providing said receiver circuit with a plurality of feedback signals. Further, Segawa does not disclose the use of a plurality of feedback signals to synchronize the receipt of data. Segawa discloses the use of a single feedback signal, also referred to as an internal oscillation signal, to phase lock the frequency of a VCO output with a carrier signal. Therefore, Segawa does not disclose a feedback circuit for providing a receiver circuit with a plurality of feedback signals based on the output of said receiver circuit to synchronize the receipt of data.

For at least these reasons, Applicants respectfully contend that Segawa does not anticipate claim 1. Applicants respectfully request the Examiner to reconsider and withdraw the rejection of claim 1 under 35 U.S.C § 102(e)

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**A2. Rejection of claim 12 under 35 U.S.C. § 102(e)**

Claim 12 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Segawa. Applicants respectfully traverse this rejection and contend that Segawa does not anticipate Claim 12.

Claim 12 is directed to a method for continuously synchronizing a source synchronous clock signal on a clock line with a data signal on a data line at a receiver of the source synchronous clock signal and the data line. The method includes the step of determining at the receiver a phase relationship between the source synchronous clock signal and the data signal each time the receiver receives the source synchronous clock signal. The method also includes the step of synchronizing the source synchronous clock signal and the data signal to be in phase at the receiver each time the receiver receives the data signal and the source synchronous clock signal. The synchronization is based on the determined phase relationship between the source synchronous clock signal and the data signal to continuously synchronize the source synchronous clock signal and the data signal to allow the receiver to integrate the data signal over an entire period of the clock signal.

Segawa does not anticipate Claim 12. Segawa does not disclose a method for continuously synchronizing a source synchronous clock signal on a clock line with a data signal on a data line at the receiver. That is, as discussed above, Segawa discloses a phase lock loop (PLL) that attempts to generate a VCO output that is phase locked to a carrier signal by comparing only the VCO output with the carrier signal. Further, as discussed above, Segawa discloses a clock signal, clock 1, as a reference for detecting the absence of a carrier signal for the mode selector circuit. As such, Segawa also fails to disclose the synchronizing of said source synchronous clock signal and said data signal to be in phase at said receiver each time said receiver receives said data signal and said source synchronous clock signal, wherein said synchronization is based on said determined phase relationship between said source synchronous clock and said source synchronous data. Nor does the Segawa reference disclose a method to allow said receiver to integrate said data signal over an entire period of said clock signal.

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In light of the above comments, Applicants respectfully submit that claim 12 of the present invention is not anticipated by, and is therefore in condition for allowance over, Segawa. Applicants respectfully request the Examiner to reconsider and withdraw the rejection of claim 12 under 35 U.S.C. § 102(e).

**B. Rejection of Claims under 35 U.S.C. § 103(a):**

Claims 8 and 23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Segawa in view of U.S. Patent No. 5,960,042 ("Chang"). Claims 10, 21, 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Segawa. For ease of the discussion below, the rejection of claims 8 and 23 under 35 U.S.C. § 103(a) are discussed separately, while rejection of claims 10, 21 and 22 under 35 U.S.C. § 103(a) will be discussed concurrently.

**B1. Rejection of Claim 8 under 35 U.S.C § 103(a)**

Claim 8 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Segawa in view of Chang. Applicants respectfully traverse this rejection and contend that neither Segawa nor Chang alone or in combination render Claim 8 unpatentable.

Claim 8 depends on independent claim 1, and therefore incorporates the patentable features of claim 1. Claim 8 characterizes the source synchronous signal as comprising a multi-level source synchronous signal.

Chang is cited as teaching a receiver for receiving multi-level signals. Chang teaches a selective call receiver used for synchronizing an internal reference to symbol edges of a plurality of symbols in a multi-level radio signal.

Neither Segawa nor Chang alone or in combination teach or suggest a receiver circuit for receiving data of a source synchronous signal and a source synchronous clock signal in a source synchronous point-to-point communication system. As distinguished from the present invention, Segawa teaches the generation of a VCO output signal that is phase locked to a carrier signal, and Chang teaches receiving multi-level signals.

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Further, both Segawa and Chang fail to teach or suggest a feedback circuit for providing a plurality of feedback signals based on an output of said receiver circuit to synchronize receipt of said data of said source synchronous signal. In contrast, Segawa teaches the use of a single feedback signal and Chang teaches receiving multilevel signals. As such, Segawa and Chang fail to teach or suggest each and every element of claim 1.

Furthermore, Segawa teaches away from a plurality of feedback signals as required by the claimed invention. Segawa is concerned with solving the inability of a conventional PLL from remaining lock after a carrier signal is lost. Conventional PLL's, as shown in figure 1 of Segawa, use a single feedback signal. Segawa teaches an additional component to the loop to allow a conventional PLL architecture to remain locked in the absence of a carrier signal. As such, Segawa teaches only one feedback signal can be used in Segawa's PLL. The present invention provides a plurality of feedback signals to synchronize receipt of data. Segawa's improvement of a conventional PLL, which only uses a single feedback signal, teaches away from the present invention, which provides a plurality of feedback signals.

For at least these reasons, Applicants respectfully submit that each and every element of claim 1 of the present invention are not taught or suggested by Segawa and Chang, and therefore Claim 8 is in condition for allowance over Segawa and Chang. Such action is kindly requested.

**B2. Rejection of Claim 23 under 35 U.S.C § 103(a)**

Claim 23 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Segawa in view of Chang. Applicants respectfully traverse this rejection and contend that neither Segawa nor Chang alone or in combination render Claim 23 unpatentable.

Claim 23 depends on independent claim 12, and therefore incorporates the patentable features of claim 1. Claim 23 characterizes the source synchronous signal as a multi-level source synchronous signal.

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Chang is cited as teaching the receiver is for receiving multi-level signals. Chang teaches a selective call receiver used for synchronizing an internal reference to symbol edges of a plurality of symbols in a multi-level radio signal.

Applicants respectfully submit that neither Segawa nor Chang, alone or in combination, teach or suggest a method continuously synchronizing a source synchronous clock signal on a clock line with a data signal on a data line at the receiver, as required by claim 12. As distinguished from the present invention, Segawa teaches the generation of a VCO output signal that is phase locked to a carrier signal, and Chang teaches receiving multi-level signals. As such, Segawa and Chang fail to teach or suggest each and every element of claim 12.

For at least these reasons, Applicants respectfully submit that each and every element of claim 12 of the present invention are not taught or suggested by Segawa and or Chang, and therefore claim 23 is in condition for allowance over Segawa and Chang. Such action is kindly requested.

**B3. Rejection of Claims 10, 21 and 22 under 35 U.S.C § 103(a)**

Claims 10, 21 and 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Segawa. Applicants respectfully traverse this rejection and contend that Segawa does not render claims 10, 21 and 22 unpatentable.

Claim 10 depends on Claim 1, and therefore incorporates the patentable features of claim 1. Claims 21 and 22 depend on claim 12, and therefore incorporate the patentable features of claim 12. Claims 10, 21 and 22 characterize the source synchronous signals as comprising differential signals.

The Examiner cites the extension of Segawa to differential signals would be obvious to one skilled in the art at the time of the invention, although, Segawa neither teaches nor suggests the use of differential signals.

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Applicants respectfully submit that Segawa neither teaches nor suggests each and every element of claims 1 or 12. More specifically, Segawa does not teach or suggest an apparatus or method for receiving data of a source synchronous signal and a source synchronous clock signal in a source synchronous point-to-point communication system. Further, Segawa fails to teach or suggest a feedback circuit for providing a plurality of feedback signals based on an output of said receiver circuit to synchronize receipt of said data of said source synchronous signal. As such, Segawa fails to teach or suggest each and every element of claims 1 and 12.

For at least these reasons, Applicants respectfully submit that each and every element of claim 1 of the present invention are not taught or suggested by Segawa, and therefore Claim 10 is in condition for allowance over Segawa. Such action is kindly requested.

**Conclusion**

In view of the above response, applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

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